IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yo Ng Zhou et al.

Assignee: Synopsys, Inc.

Title: SYSTEM AND METHOD FOR SIMULATION OF AN INTEGRATED CIRCUIT DESIGN USING A HIERARCHICAL INPUT NETLIST AND DIVISIONS ALONG HIERARCHICAL BOUNDARIES THEROF

Serial No.: 09/808,339 File Date: March 13, 2001

Examiner: Thai Q. Phan Art Unit: 2128

Docket No.: SYN-0176

Date: April 30, 2004

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT IN RESPONSE TO THE FIRST OFFICE ACTION

Initial Comments

Claims 1, 3-15, and 17-23 are pending in the present application. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,339,836 (Eisenhofer).

Claims 1 and 15 are amended. Claims 2 and 16 are cancelled.